REMARKS

Claims 1-3, 24-29, and 33-39 remain in this application. No claims have been added or cancelled. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

Claim Rejection - 35 U.S.C. § 102

The Examiner has rejected claims 1-3, 24-29, and 33-39 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,367,690 to Schiffleger (hereinafter "Schiffleger"). The Applicants respectfully submit that the present claims are not anticipated by Schiffleger.

Claim 1 recites a method comprising "*requesting access to a resource for a first process, **the first process having a corresponding first semaphore**; determining whether the resource is being accessed by a second process, **the second process having a corresponding second semaphore**; and denying the first process access to the resource if the resource is being accessed by the second process as indicated by a lock on the resource, wherein the lock is indicated at the second semaphore*". Schiffleger does not teach or suggest these limitations.

As discussed in paragraph [0006] of the patent application, "*[t]he classical approach ... is to implement a semaphore for each resource*". In contrast, claim 1 provides that the first semaphore corresponds to the first process and the second semaphore corresponds to the second process. FIG. 2 of the patent application shows a system in which each resource has a corresponding semaphore, whereas FIG 3 of the patent application shows a system in which each process has a corresponding semaphore system. There is a difference.

Schiffleger discusses communication between processors in a multiprocessor system (see e.g., the Title and the Field of the Invention). As discussed at column 4, lines 3-11, FIG. 1 illustrates a high-level block diagram of the tightly coupled multiprocessor communication system 200 within a multiprocessor data processing system. Processors 202.1 through 202.N are connected to local control circuits 10.1 through 10.N, respectively. Local control circuits 10.1 through 10.N are connected in turn to shared resource circuit 70. As discussed at column 5, lines 16-18, local control circuits 10.1 through 10.N arbitrate among themselves to prevent more than one access to shared resource circuit 70 at a time. FIG. 3 shows an electrical block diagram of the local control circuit 10 of FIG. 1. Shown is local semaphore register 18. A description of how the local semaphore register 18 is used is provided at column 6, lines 15-44 (with emphasis added):

> "...processor 202 registers the cluster number and requests and loads the semaphore register associated with that cluster into its local semaphore register 18. From that point on, the local control circuit 10 associated with that processor 202 maintains a **copy** of the assigned cluster's shared semaphore register in its local semaphore register 18.
>
> Shared semaphore registers are used to synchronize activity and to restrict access to shared information registers. In one typical operation, an access to shared information registers begins with processor 202 issuing a "test and set" command to local control circuit 10. Local control circuit 10 then checks the status of the appropriate bit in its local semaphore register 18. If the bit is set, then another processor has control of that shared register and processor 202 waits for the bit to be cleared. If the bit is not set, local control circuit 10 asserts its CPU_In_Progress line 32 to each of the shared resource subcircuits 71 and sends a command to set the bit in the semaphore register for that cluster.
>
> By software convention, setting a bit in the shared semaphore register grants control circuit 10 access to the associated shared information register. Control circuit 10 then has exclusive control to read or write that register. Upon finishing, control circuit 10 clears the set semaphore bit and another processor can access the register."

Accordingly, shared semaphore registers are used to restrict access to shared information registers. Applicants respectfully submit that the shared information registers have corresponding shared semaphore registers. Each processor 202 has a

connected local control circuit 10 that has a local semaphore register that is only a **copy** of the shared semaphore register. Accordingly, Applicants submit that each of the local semaphore registers 18 correspond to the shared resource. In other words, rather than having just one corresponding semaphore for a shared resource Schiffleger discusses additionally having multiple copies of said one corresponding semaphore for the shared resource but located closer to the processors. This is different from what is being claimed in claim 1.

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference. The Federal Circuit has indicated that the standard for measuring lack of novelty by anticipation is strict identity. "*For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference.*" In Re Bond, 910 F.2d 831, 15 USPQ.2d 1566 (Fed. Cir. 1990).

For at least these reasons, claim 1 is believed to be allowable over Schiffleger. Claims 2-3, and 33 depend from claim 1 and are believed to be allowable therefor, as well as for the recitations set forth in each of these dependent claims.

Independent claims 24, 27, and 36, as well as each of these independent claims respective dependent claims, are also believed to be allowable.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 2/16/06

Brent E. Vecchia
Reg. No. 48,011

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1030
(303) 740-1980